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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,316	06/05/2001	Louis Jacobus Botha	RONI005/00US	5717

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COOLEY GODWARD LLP
ATTN: PATENT GROUP
11951 FREEDOM DRIVE, SUITE 1700
ONE FREEDOM SQUARE- RESTON TOWN CENTER
RESTON, VA 20190-5061

EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2664	12

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/873,316	Applicant(s) Louis J. Botha
	Examiner Ho	Art Unit 2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 22, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *11*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The amendment filed 07/22/03 have been entered and made of record.

2. Applicant's amendment with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection...

3. Claims 1-14 are pending.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> > (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claim 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita (U.S.Patent No. 6,564,343 B1).

In the claim 1, see figure 1, Yamashita discloses a bit deinterleave circuit comprises:....a first deinleave unit for deinterleaving the received signal completing a bit interleave process; and

second deinterleave unit for rearranging command signals to output the command signals according to a signal output by the first deinterleave unit (see abstract) ; comprising:

- a memory buffer (RAM# 42#0 and 42#1; RAMs 110#0 and 110#1) to store the data (see figure 3, col. 6, lines 55-67);
- coupled to memory buffer (see figure 3, col. 6, lines 55-67) , for performing a first and second de-interleaving (see figure 1, col. 5, lines 43-47) of the data in memory buffer, wherein said includes means for reading and writing the data to the memory buffer in connection with first and second deinterleaving (see col. 5, lines 43-47, col. 6, lines 55-67).

6. In the claim 6, see figure 1, Yamashita discloses a bit deinterleave circuit comprises:....a first deinleave unit for deinterleaving the received signal completing a bit interleave process; and second deinterleave unit for rearranging command signals to output the command signals according to a signal output by the first deinterleave unit (see abstract) ; comprising:

- a memory buffer (RAM# 42#0 and 42#1; RAMs 110#0 and 110#1) to store the data (see figure 3, col. 6, lines 55-67);
- coupled to memory buffer (see figure 3, col. 6, lines 55-67) , for performing a first and second de-interleaving (see figure 1, col. 5, lines 43-47) of the data in memory buffer, wherein said includes means for reading and writing the data to the memory buffer in connection with first and second deinterleaving (see col. 5, lines 43-47, col. 6, lines 55-67).

7. In the claims 9, 11, 13, see figure 1, Yamashita discloses a bit deinterleave circuit comprises:....a first deinleave unit for deinterleaving the received signal completing a bit interleave process; and second deinterleave unit for rearranging command signals to output the command signals according to a signal output by the first deinterleave unit (see abstract) ; comprising:

- a memory buffer (RAM# 42#0 and 42#1; RAMs 110#0 and 110#1) to store the data (see col. 5, lines 43-47, col. 6, lines 55-67);
- coupled to memory buffer (RAM# 42#0 and 42#1; RAMs 110#0 and 110#1) , for performing a first and second de-interleaving (see figure 1) of the data in memory buffer (see col. 6, lines 55-67).

8. In the claims 2, 10, Yamashita discloses second de-interleaving as the data is written to memory buffer and performs first de-interleaving as stored data is read from memory buffer (see col. 5, lines 43-47, col. 6, lines 55-67).

9. In the claim 3, Yamashita discloses memory buffer stores the data, and wherein said means performed said first and second de-interleaving as the stored data is read from memory buffer (see col. 5, lines 43-47, col. 6, lines 55-67).

10. In the claims 4, 7, Yamashita discloses the data comprises radio frames, memory buffer comprises a plurality of radio frame blocks, and said means causes radio frames to be stored in radio frame blocks (see col. 5, lines 43-47, col. 6, lines 55-67).

11. In the claims 5, 8, Yamashita discloses the data is transmitted over one or more physical channels, wherein each of radio frames comprises a physical channel frame associated with each physical channel, each of radio frame blocks comprises a physical channel block associated with each physical channel, and said means causes said physical channel frames to be stored in said physical channel blocks (see col. 11, lines 55-67, col. 12, lines 1-50).

12. In the claim 12, Yamashita discloses reassembling one or more physical channels from the data stored in memory buffer; performing a second removal of discontinuous transmission indication bits from the data stored in memory buffer; demultiplexing the data stored in memory buffer into a plurality of transport channels; and reassembling transport block from the data stored in memory buffer, wherein the data comprises radio frames. (See col. 12, lines 55-67, col. 13, lines 1-35).

13. In the claim 14, Yamashita discloses reassembling one or more physical channels from the data stored in said memory buffer; performing a second removal of discontinous transmission indication bits from the data stored in memory buffer; demultiplexing the data stored in memory buffer into a plurality of transport channels; and reassembling transport blocks from the data stored in memory buffer wherein the data comprises radio frames (see col. 11, lines 55-67, col. 12, lines 1-50).

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Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong Ho whose telephone number is (703)306-4529. The examiner can normally be reached on Monday-Friday from 9am to 3pm.

15. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington, Chin, can be reached on (703)305-4633.

Any inquiry of a general nature or relating to the status of this application or proceeding should be direct to the group receptionist whose telephone number is (703) 305-3900.

CH

Date 09-23-03..